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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,747	03/03/2004	John M. Lauffer	200300168-1	2917

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,747	LAUFFER ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 PGS*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election of Group I, claims 1-17, in the reply filed on 3/20/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 and 8-16 rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al. (US 6353189).

Regarding claim 1, as shown in figure 1, Shimada et al. disclose a circuitized substrate comprising:

(a) At least one dielectric layer 5 (column 21, line 12) having first and second opposing sides;

(b) a conductive ground plane 6 (column 11, line 9 and 25-33) located on the first opposing side of the dielectric layer;

(c) at least one conductive signal line 1 (column 11, line 6) located on the second opposing side of the dielectric layer; and

(d) first and second conductive ground lines 2 (shield pattern, column 21, line 6) located on the second opposing side of the dielectric layer on opposite sides of the at

least one conductive signal line and electrically coupled to the ground plane located on the first opposing side of the dielectric layer, the first and second conductive ground lines providing shielding for the at least one conductive signal line during the passage of electrical current through the signal line (column 21, lines 26-33).

Regarding claim 2, Shimada et al. disclose the dielectric layer is selected from the group consisting of fiberglass-reinforced polymer resin (prepreg, column 21, line 21). It is noticed that, prepreg sheet can be formed of fiberglass-reinforced polymer resin (a glass epoxy resin, see column 22, lines 4-5).

Regarding claim 3, Shimada et al. disclose the at least one conductive plane is comprised of copper (metallic material, including copper column 9, lines 11-13).

Regarding claim 4, Shimada et al. disclose the at least one conductive signal line is comprised of copper (column 21, line 18 and metallic material in column 9, lines 11-13).

Regarding claim 5, Shimada et al. disclose the first and second ground lines are each comprised of copper (metallic material, column 9, lines 11-13).

Regarding claim 6, as clearly shown in figure 1, Shimada et al. disclose every limitation as shown in claim 1 above and further include first, second, and third conductive thru-holes 7a/7b (conductive pillars, arbitrary selecting any conductive pillars), the first and third conductive thru-holes electrically couple the first and second conductive ground lines 2 to the conductive ground plane, see column 21, lines 26-33.

Regarding claim 8, Shimada et al. disclose every limitation as shown in claim 4 above including signal line is comprised of copper.

Regarding claim 9, Shimada et al. disclose every limitation as shown in claim 1 above and include additional dielectric and conductive layers as part thereof (it's a multilayer printed circuit board).

Regarding claim 10, Shimada et al. disclose every limitation as shown in claim 9 above and include first and second pluralities of external conductive pads located on opposite sides of the circuitized substrate for electrically coupling the circuitized substrate to external electrical components (see figure 20).

Regarding claim 11, Shimada et al. disclose the circuitized substrate is a chip carrier. It is noticed that multi-chip module is used for surface mounting chips or chip carriers (semiconductor package, column 21, lines 48-49).

Regarding claim 12, Shimada et al. disclose the circuitized substrate is a printed circuit board (column 31, line 16).

Regarding claim 13, Shimada et al. disclose every limitation as shown in claim 1 above including an electrical component (a semiconductor device) electrically coupled to the circuit board (see column 21, lines 47-51).

Regarding claim 14, Shimada et al. disclose the electrical component is a chip carrier. It is noticed that multi-chip module is used for surface mounting chips or chip carriers (semiconductor package, column 21, lines 48-49).

Regarding claim 15, Shimada et al. disclose the electrical component is a semiconductor chip carrier (see semiconductor package, column 21, lines 48-49).

Regarding claim 16, Shimada et al. disclose every limitation as shown in claim 6 above including first, second, and third conductive thru-holes 7a/7b, the first and third

conductive thru-holes electrically couple the first and second conductive ground lines 2 to the conductive ground plane, see column 21, lines 26-33.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 7 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. in view of Ishizuki et al. (US 20040009666).

Regarding claims 7 and 17, as shown in figure 1, Shimada et al. disclose every limitation as shown in claim 6 above and further include a second dielectric layer 9 (column 21, lines 14-15) located on the conductive ground plane 6 opposite the first dielectric layer.

However, Shimada et al. failed to disclose a second conductive signal line located on the second dielectric layer 9 on a side thereof opposite the conductive

ground plane, and the second conductive thru-hole electrically coupling the at least one conductive signal line to the second conductive signal line.

It is conventionally well known in the art that signal lines are formed on a plurality of insulator layers in a printed circuit board, and selected/predetermined signal lines formed on different surfaces are electrically interconnected by conductive via(s). At least in figure 28, Shimada et al. discloses signals lines formed on a plurality of insulator layers; therefore, at least a second conductive signal line is located on the second dielectric layer 9 and it is part of a circuitry arrangement.

Ishizuki et al., as shown in figures 1I and 4, teach a multilayer circuitized substrate comprising a signal line 7 (conductive member, paragraph 40) formed on an insulating layer (no number). At least a grounding layer 3 (conductive layer, paragraph 37; also see abstract and paragraph 11) formed on opposite side of the insulating layer, shielding wall 8 (side wall, paragraph 41) formed on both sides of the signal line 7 and electrically connected to the grounding layer 3. Signals lines 31/52 (paragraph 49) are formed on both surfaces of the substrate and at least one of the signal lines 51 is electrically connected to the signal line 7 by conductive via 52 (paragraph 49) penetrating through the insulating layers and the ground layer 3.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the teaching(s) from Ishizuki et al. to arrange the second conductive thru-hole like 7a electrically coupling the at least one conductive signal line to the second conductive signal line in order for the at least one conductive signal line to

electrically connect other components formed within the circuit board in a shortest distance, which in part optimizing electric resistance within a signal path.

Citation of Relevant Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kobayashi et al. (US 6040524) disclose a printed circuit board having two holes connecting first and second ground areas.

Teshome et al. (US 6236572) disclose a controlled impedance bus and method for a computer system.

Sasaoka et al. (US 6010769) disclose a multilayer wiring board and method for forming the same.

Andry (US 5662816) discloses a signal isolating microwave splitters/combiners.

Ohshima et al. (US 5455393) disclose a multilayered printed wiring board and method of manufacturing the same.

Van Dyke et al. (US 6657130) disclose an electrical and physical design integration method and apparatus for providing interconnections on first level ceramic chip carrier packages.

Peters et al. (US 6239485) disclose a reduced cross-talk noise high density signal interposer with power and ground wrap.

Oprysko et al. (US 6992255) disclose a via and via landing structures for smoothing transitions in multi-layer substrates.

Anstrom et al. (US 6495772) disclose a high performance dense wire for printed circuit board.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
6/7/06

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